Attorney's Docket No.: 12732-026001 / US4850

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jun KOYAMA et al. Art Unit: Unknown Serial No.: Not yet assigned Examiner: Unknown

Filed : April 17, 2001

Title : SELF-LUMINOUS DEVICE AND ELECTRIC MACHINE USING THE SAME

Commissioner for Patents Washington, D.C. 20231

## PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the specification:

Replace the paragraph beginning at page 26, line 16 with the following rewritten paragraph:

Specifications of the FPC input terminals used in this embodiment are shown in Table 1. Note that the "terminal Nos." in Table 1 correspond to the numbers (1 to 100) above the FPC input portions (1) 904a and the FPC input portions (2) 904b in Fig. 9.

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<i>i</i> .	symbol of treminal	valtage (range)[V]	remarks (name of signal etc.)
1	EL_CATH		pad (dummy terminal)
2		approximately 4 (0.0~9.0)/9	EL driving direct current power supply (positive terminal)
3	EL ANOD	9	EL driving direct current power supply (negative terminal)
4	S LATE S LAT	0.0 / 9.0	latch inversion signal of source driver circuit
5		0.0/9.0	latch signal of source driver circuit
6	VD_16	0.0 / 9.0	digital video signal 16
7	VD 15 VD 14	0.0/9.0	digital video signal 15
8	VD_13	0.0 / 9.0	digital video signal 14
9	VD 12	0.0 / 9.0 0.0 / 9.0	digital video signal 13
10	VD 11	0.0/9.0	digital video signal 12
11	VD 10		digital video signal 11
12	VD_09	0.0 / 9.0	digraal video signal 10
13	VD 08	0.0 / 9.0	digital video signal 9
14	VD_07	0.0 / 9.0	digital video signal 8
15		0.0 / 9.0	digital video signal 7
16	VD 06 VD 05	0.0/9.0 0.0/9.0	digital video signal 6
17	VD 04	0.0/9.0	digital video signal 5
18	VD_03 -		digital video signal 4
	<u>∨D.03</u> - ∨D.02	0.0/9.0 0.0/9.0	digital video signal 3 -
19	VD 01	0.0 / 9.0	digital video signal 2
21	S GND	0.02 9.0	digital video signal 1
22	SVDD	9	negative power supply of source driver circuit positive power supply of source driver circuit
23	S_LEFT -	0.0 or 9.0	
23	JLEFI -	0.0 or 9.0	switching of scanning direction of source-driver circuit (0.0: scanning
24	S_SP	0.0/9.0	to the right, 9.0: scanning to the left)
25	S_CKb	0.0 / 9.0	start pulse of source driver circuit Inverted clock signal of source driver circuit
26	S_CK	0.0 / 9.0	clock signal of source driver circuit
27	VD_01	0.0 / 9.0	digital video signal 1
5 28	VD_02	0.0 / 9.0	digital video signal 2
29	VD_03	0.0 / 9.0	digital video signal 3
30	VD_04	0.0 / 9.0	digital video signal 4
31	VD_05	0.0 / 9.0	digital video signal 5
32	VD_06	0.0 / 9.0	digital video signal 6
33	VD_07	0.0 / 9.0	digital video signal 7
34	VD_08	0.0 / 9.0	digital video signal 8
35	VD_09	0.0 / 9.0	digital video signal 9
36	VD 10	0.0 / 9.0	digital video signal 10
37	VD_11	0.0 > 9.0	digital video signal 11
38 -	VD_12	0.0 / 9.0	digital video signal 12
39 -	VD_13	0.0 / 9.0	digital video signal 12
40	VD_13	0.0 / 9.0	digital video signal 13
41	VD_15	0.0 / 9.0	digital video signal 15
42	VD_16	0.0/9.0	f
43	G_GND	0.07 9.0	digital video signal 16 negative power supply of gate driver circuit
43 -	G_VDD	10 -	positive power supply of gate driver circuit
45	G_UP	0.0 or 10.0	switching of scanning direction of gate driver circuit (0.0: scanning to
40	G_UF	0.0 or 10.0	the right, 9.0: scanning to the left)
46	C CIV	0.0/10.0	· · · · · · · · · · · · · · · · · · ·
46	G_CKb G_CK	0.0 / 10.0	inverted clock signal of gate driver circuit
	G SP	0.0 / 10.0	clock signal of gate driver circuit start pulse of gate driver circuit
48		9	EL driving direct current power supply (positive terminal)
<u>49</u>	EL ANOD		
50	EL CATH	approximately 4 (0.0~3.0)/9	EL driving direct current power supply (negative terminal) pad (dummy terminal)

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Replace the paragraph beginning at page 27, line 10 with the following rewritten paragraph:

Table 2 shows the size of TFTs included in the shift register, the NAND circuits, and the buffers which constitute the gate driver circuits of this embodiment. The shift register, the NAND circuits, and the buffers use p-channel TFTs and n-channel TFTs, and both of them are shown in Table 2. The symbols in Table 2 correspond to reference symbols of Fig. 11.  $L[\mu m]$  in Table 2 represents the channel length of the TFT whereas  $W[\mu m]$  represents the channel width of the TFT.

Pch-TFT	L[µm]	W[µm]	Nch-TFT	L[µm]	Lov[µm]	W[μm]
g chsw_a	- 4.5	20	g_chsw_a	5	0.5	10
g sftr b	4.5	16	g_sftr_b	5	0,5	8
g_sftr_c	4.5	40	g sftr c	5	0.5	20
g sftr_d	4.5	10	g_sftr_d	5	0.5	5
	- 4.5	22	g nand_e	5	0.5	22
g nand_e g buff_f	4.5	50	g_buff_f	5	0.5	25

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Replace the paragraph beginning at page 28, line 8, with the following rewritten paragraph:

Table 3 shows the size of TFTs included in the shift register, the NAND circuits, and the buffers which constitute the source driver circuit of this embodiment. The shift register, the NAND circuits, and the buffers use p-channel TFTs and n-channel TFTs, and both of them are shown in Table 3. The symbols in Table 3 correspond to the reference symbols of Fig. 12.  $L[\mu m]$  in Table 3 represents the channel length of the TFT whereas  $W[\mu m]$  represents the channel width of the TFT. The channel length of the n-channel TFT includes an LOV region.

Pch-TFT	L[µm]	W[µm]	Nch-TFT	L[µm]	Lov[µm]	W[μm]
s_chsw_a	- 4.5	60	s_chsw_a	5	0.5	40
s_sftr_b	4.5	50	s_sftr_b	5	0.5	25
s_sftr_c	4.5	100	s_sftr_c	5	0.5	50
s_sftr_d	4.5	30	s_sftr_d	5	0.5	15
s_nand_e	4.5	50	s_nand_e	5	0.5	50
s_buf1_f	4.5	100	s_buf1_f	5	0.5	50
s_buf1_g	4.5	100	s_buf1_g	5	0.5	50
s_buf1_h	4.5	300	s_buf1_h	5	0.5	150
s_buf1_i	4.5	400	s_buf1_i	5	0.5	200
s_lat1_j	4.5	16	s_lat1_j	5	0.5	8
s_lat1_k	4.5	16	s lat1 k	5	0.5	8
s lat1_m	4.5	4	s_lat1_m	5	0.5	2
s_buf2_n	4.5	30	s_buf2_n	5	0.5	15
s_lat2_p	4.5	16	s_lat2_p	5	მ.5	8
s lat2 r	4.5	16	s_lat2_r	5	0.5	8
s_lat2_s	4.5	4	s_lat2_s	5	0.5	2
s_buf3_t	4.5	30	s_buf3_t	5	0.5	15

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Replace the paragraph beginning at page 28, line 23 and continuing to page 29, line 3 with the following rewritten paragraph:

Specifications of the display panel according to this embodiment are shown in Table 4.

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size of screen	diagonal 4.0 inches
number of pixels	640×480
interval of pixels	126 µ m
grey scales	64 (6bit)
aperture ratio	60%
operating clock frequency of source driver circuit	12. 5MHz
operating clock frequency of gate driver circuit	252kHz
voltage of driver circuit	12V
voltage of display region	6V
duty ratio	61.5%
color	monochrome

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Replace the paragraph beginning at page 58, line 20, with the following rewritten paragraph:

The molecular formula of the EL material (coumarin pigment) reported in the above article is shown below.

Replace the paragraph beginning at page 59, line 3, with the following rewritten paragraph:

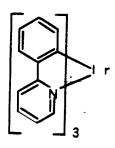
The molecular formula of the EL material (Pt complex) reported in the above article is shown below.

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Replace the paragraph beginning at page 59, line 12, with the following rewritten paragraph:

The molecular formula of the EL material (lr complex) reported in the above article is shown below.



#### In the claims:

- 4. (Amended) A self-luminous device according to claim 1, wherein the source region and the separate semiconductor film are electrically connected to their respective power supply lines.
- 5. (Amended) A self-luminous device according to claim 1, wherein the separate semiconductor film has a region that overlaps with the gate electrode with the gate insulating film sandwiched therebetween, and the region overlapping with the gate electrode takes up 60% or more of the separate semiconductor film.

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### **REMARKS**

Claims 1-26 are pending in this application with claims 1, 11, 14, 19, and 23 being independent. Claims 4 and 5 have been amended to place the application in better condition for initial examination. No new matter has been added.

Attached is a marked-up version of the changes being made by the current amendment. The attached page is captioned <u>"Version with markings to show changes made."</u>

The examiner is invited to contact the undersigned with any questions at the number set forth below. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: April 17, 2001

William D. Hare Reg. No. 44,739

Fish & Richardson P.C. 601 Thirteenth Street, NW Washington, DC 20005 Telephone: (202) 783-5070

Facsimile: (202) 783-2331

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# Version with markings to show changes made

# In the specification:

The paragraph beginning at page 26, line 16 has been amended as follows:

Specifications of the FPC input terminals used in this embodiment are shown in Table 1. Note that the "terminal Nos." in Table 1 correspond to the numbers (1 to 100) above the FPC input portions (1) 904a and the FPC input portions (2) 904b in Fig. 9.

[[Table 1]]

	symbol of transpol	Valtage (mage) [V]	remarks (name of same) etc.)
1			and (during turned)
<del></del>	EL CATH	4 (0.0~9.0)/9	EL driving direct ourrent power punch (pending terminal)
- 1	EL ANOD		TEL GROUP GROUP SUPPLY SUPPLY (DESIGNATION TAYMOND)
	SLATE	0.0/9.0	lieton inversion signal of source driver circuit
	SLAT	0.0/9.0	latch signal of source driver circuit
	VD 16 VD 15	0.0 / 9.0	digital video signel 16
	VD 14	0.0/9.0	digital video sumel 15
8	VD 13	0.0/0.0	digital video signel 14
		0.0/9.0	distrati video signet 13
10	VD 12	0.0/0.0	distal video signal 12
11	~ VD 10	0.0/0.0	distal video signal [1]
12	VD 00	0.0/9.0	distal video signal 10
13	VD 08	0.0/9.0	duttal video sumal 9
14	VD 07		digital video signel \$
15	VD 06	0.0/9.0	distal video signel ?
16	VD.06	0.0/1.0	diartal video surrei 6
17	VD 04	0.0/1.0	distal video signal 5
18	VD 03	0.0/1.0	diartal video signel 4
19	VO.02	0.0/1.0	diatal video signel 3
20	VD 01	0.0/1.0	distal video sisnel 2
21	S GND	0	detal video senel !
22	\$.V00		negative power supply of source driver circuit
23	SLEFT	0.0 or 9.0	positive power supply of source driver circuit
	٠,٠٠٠	U.U GF 9.U	switching of scanning direction of squirce driver circuit (0.0: scene
24	S.SP	0.0/1.0	to the right, 9.0 scenning to the left)
25	S CROS	0.0/0.0	start pulse of source driver circuit
26	S.CK	0.0/1.0	inverted clock sumsi of source driver circuit
27	VD 01	0.0/1.0	clock sumet of source driver circuit
23	VD 02	0.0/1.0	dustal video sumal 1 dustal video sumal 2
29	VD 03	0.0/9.0	detai video signal 3
30	VD 04	0.0/9.0	durtal video sumei 4
31	VD.06	0.0/1.0	digital video signel 5
32	VD 06	0.0/1.0	digital video signel 6
33	VD 07	0.0/9.0	destal video signal 7
34	VD 08	0.0/9.0	destal video signel 8
35	VD 00	0.0/9.0	destal video sumei 9
34	VD 10	0.0/9.0	digital video signel 10
37	VD 11	0.0/9.0	distal video signel 11
38	VD 12	0.0 / 9.0	digital video signel 12
39	VD 13	0.0/9.0	digital video signal 13
40	V0 14	0.0 2.0	digital video signal 14
41	VD 15	0.0 / 9.0	digital video signel 15
42	VD 16	0.0 / 9.0	digital video signel 18
43	G GND	0.07.07	negative power supply of gate driver circuit
44	Q VDD	10	positive power supply of gate driver circuit
45	G UP	0.0 or 10.0 ·	switching of scanning direction of gate driver circuit (0.0: scanning
-	4.5	and 100 .	
44	G.CHO.	0.0/10.0	the right, \$.0 segment to the left) inverted clock segral of sets driver eresit
47	G CK	0.0/10.0	clock surrel of sets driver current
48	G SP	0.0/10.0	start pulse of sets driver careait
44	EL ANOO	1	EL driving dreet gurrent sever supply (seedove terminal)
50			EL driving direct current power supply (negative terminal)
			ped (durany terreral)

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The paragraph beginning at page 27, line 10 has been amended as follows:

Table 2 shows the size of TFTs included in the shift register, the NAND circuits, and the buffers which constitute the gate driver circuits of this embodiment. The shift register, the NAND circuits, and the buffers use p-channel TFTs and n-channel TFTs, and both of them are shown in Table 2. The symbols in Table 2 correspond to reference symbols of Fig. 11. L[µm] in Table 2 represents the channel length of the TFT whereas W[µm] represents the channel width of the TFT.

## [[Table 2]]

Pch-TFT	L[µm]	W[µm]	Nch-TFT	L[µm]	Lov[µm]	W[μm]
g_chsw_a	4.5	20	g chsw a	5	0.5	10
g_sftr_b	4.5	16	g_sftr_b	5	0.5	
g sftr c	4.5	40	g_sftr_c	5	0.5	30
g_sftr_d	4.5	10	g sftr d	5	0.5	
g_nand_e	4.5	22	g nand e	5	0.5	
g_buff_f	4.5	50	g buff f	5	0.5	22 25

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The paragraph beginning at page 28, line 18, has been amended as follows:

Table 3 shows the size of TFTs included in the shift register, the NAND circuits, and the buffers which constitute the source driver circuit of this embodiment. The shift register, the NAND circuits, and the buffers use p-channel TFTs and n-channel TFTs, and both of them are shown in Table 3. The symbols in Table 3 correspond to the reference symbols of Fig. 12.  $L[\mu m]$  in Table 3 represents the channel length of the TFT whereas  $W[\mu m]$  represents the channel width of the TFT. The channel length of the n-channel TFT includes an LOV region.

[[Table 3]]

Pch-TFT	L[ <i>μ</i> m]	W[μm]	Nch-TFT	L[µm]	Lov[#m]	W(μm
s_chsw_a	4.5	60	s_chsw_a	5	0.5	40
s_sftr_b-	4.5	50	s_sftr_b	5	0.5 -	25
s_sftr_c ¯	4.5	100	s_sftr_c	5	0.5	50
s_sftr_d-	4.5	30	s_sftr_d	5	0.5 -	15
s_nand_e	4 5	50	s_nand_e	5	0.5	50
s_buf1_f	4.5	100	s_buf1_f	5	0.5	50
s_buf1_g	4.5	100	s buf1 g	5	0.5	50
s_buf1_h	4.5	300	s_buf1_h	5	0.5	150
s_buf1_i	4.5	400	s_buf1_i	5	0.5	200
s_lat1_	4.5	16	s_lat1_j	5	0.5	8
s_lat1_k	4.5	16	s lat1 k	5	0.5	8
s_lat1_m	4.5	4	s_lat1_m	5	0.5	2
s_buf2_n	4.5	30	s_buf2_n	5	0.5	15
s lat2 p	4.5	16	s_lat2_p	5	0.5	8
s_lat2_r	4.5	16	s_lat2_r	5	0.5	8
s lat2 s	4.5	4	s_lat2_s	5	0.5	2
s_buf3_t	4.5	30	s_buf3_t	5	0.5	15

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The paragraph beginning at page 28, line 23 and continuing to page 29, line 3 has been amended as follows:

Specifications of the display panel according to this embodiment are shown in Table 4. **[[Table 4]]** 

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size of screen	diagonal 4.0 inches
number of pixels	640×480
interval of pixels	126 µ m
grey scales	64 (6bit)
aperture ratio	60%
operating clock frequency of source driver circuit	12. 5MHz
operating clock frequency of gate driver circuit	252kHz
voltage of driver circuit	12V
voltage of display region	6V
duty ratio	61.5%
color	monochrome

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The paragraph beginning at page 58, line 20, has been amended as follows:

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The molecular formula of the EL material (coumarin pigment) reported in the above article is shown below.

## [[Chemical formula 1]]

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The paragraph beginning at page 58, line 24, has been amended as follows:

The molecular formula of the EL material (Pt complex) reported in the above article is shown below.

# [[Chemical formula 2]]

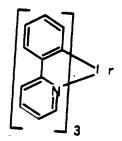
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The paragraph beginning at page 59, line 12, has been amended as follows:

The molecular formula of the EL material (lr complex) reported in the above article is shown below.

[[Chemical formula 3]]



### In the claims:

- 4. (Amended) A self-luminous device according to [claim1] claim 1, wherein the source region and the separate semiconductor film are electrically connected to their respective power supply lines.
- 5. (Amended) A self-luminous device according to [claim1] claim 1, wherein the separate semiconductor film has a region that overlaps with the gate electrode with the gate insulating film sandwiched therebetween, and the region overlapping with the gate electrode takes up 60% or more of the separate semiconductor film.